

FIG. 1(a) (Background Art)

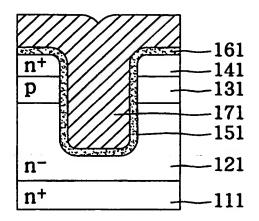


FIG. 1(b) (Background Art)

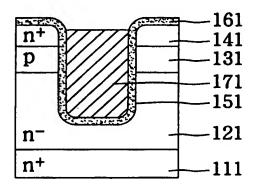


FIG. 1(c) (Background Art)

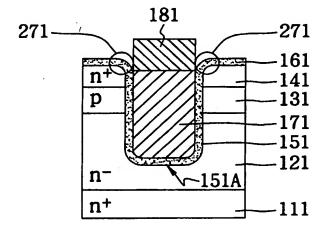


FIG. 1(d) (Background Art)

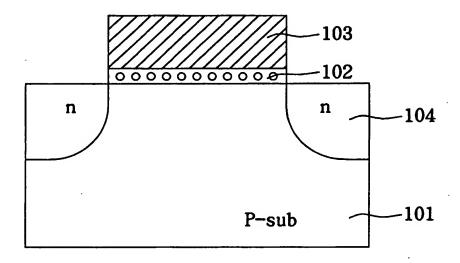


FIG. 1(e) (Background Art)

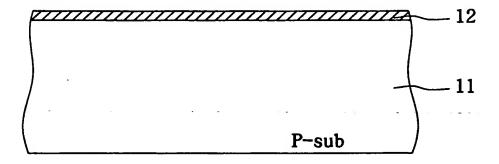


FIG. 2

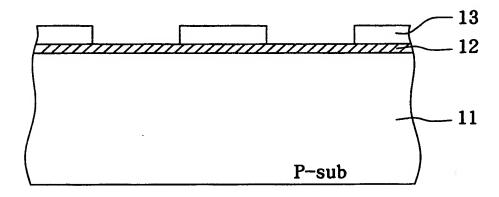


FIG. 3

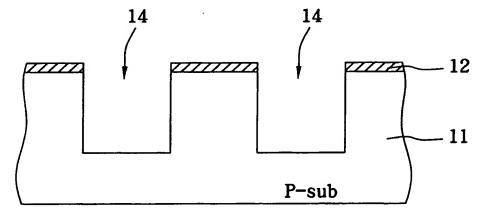
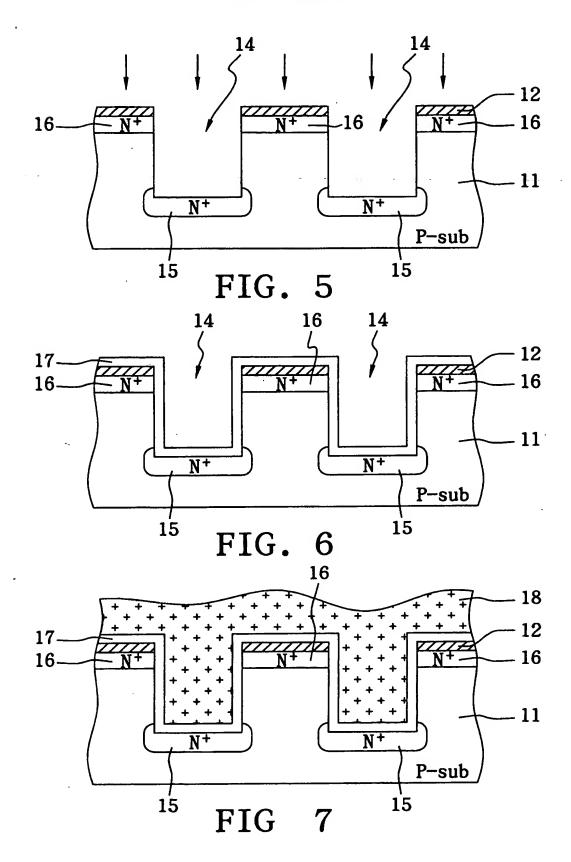


FIG. 4

NON-VOLATILE MEMORY ARRAY HAVING VERTICAL TRANSISTORS AND MANUFACTURING METHOD THEREOF Application No. [New] – Attorney Doc. No. LEE.002 Inventor: Shone FUJA



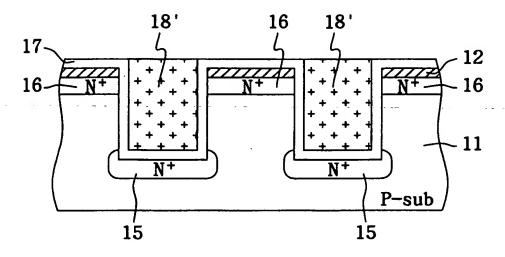


FIG. 8

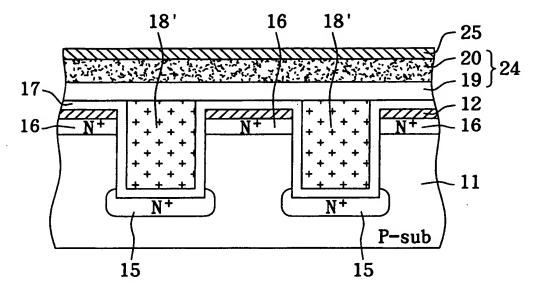


FIG. 9

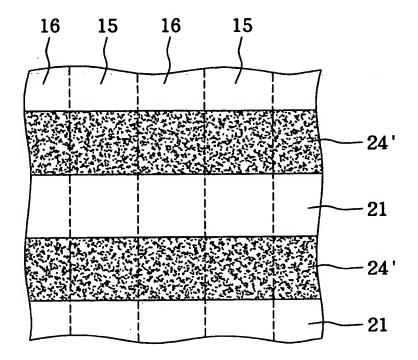


FIG. 10

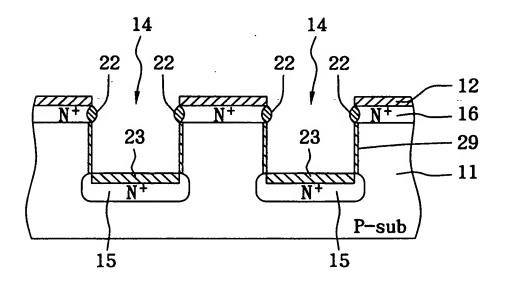


FIG. 11

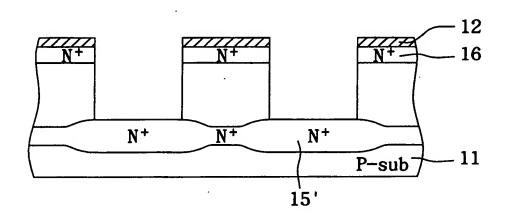


FIG. 12

NON-VOLATILE MEMORY ARRAY HAVING VERTICAL TRANSISTORS AND MANUFACTURING METHOD THEREOF Application No. [New] - Attorney Doc. No. LEE.002 Inventor: Shone FUJA

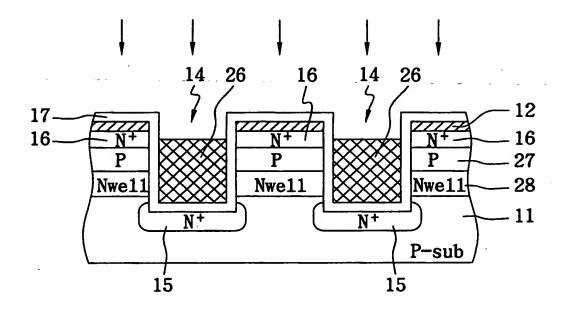


FIG. 13

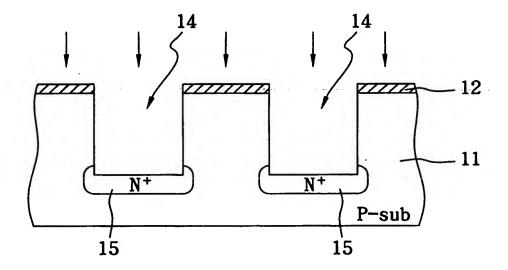


FIG. 14

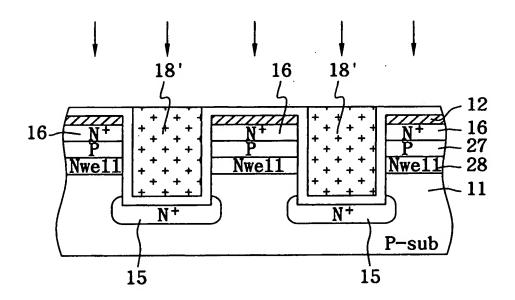


FIG 15

NON-VOLATILE MEMORY ARRAY HAVING VERTICAL TRANSISTORS AND MANUFACTURING METHOD THEREOF Application No. [New] – Attorney Doc. No. LEE.002 Inventor: Shone FUJA

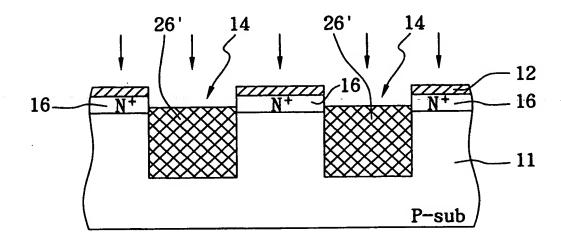


FIG. 16

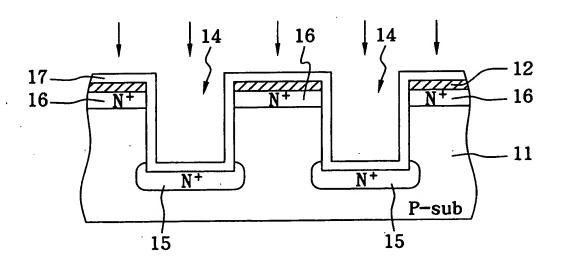


FIG. 17

NON-VOLATILE MEMORY ARRAY HAVING VERTICAL TRANSISTORS AND MANUFACTURING METHOD THEREOF Application No. [New] -- Attorney Doc. No. LEE.002 Inventor: Shone FUJA

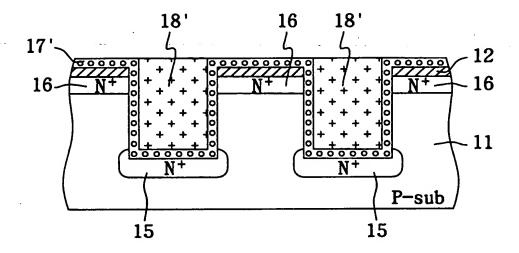


FIG. 18